GOC-QF040 V1.3

Bluetooth Module Hardware Specification

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NOTES:

1.The module must use ladder steel net, and recommend ladder steel net thickness 0.16--0.20mm. The adaptability of the products is adjusted accordingly.
2.Before the use of the module, bake at 60 degrees centigrade and bake for 12 hours.

Release Record

Version Number	Date	Comments
V1.0	2020/12/17	Initial draft

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1. Introduction

GOC-QF040 is a system on-chip (SoC) with on-chip Bluetooth, audio and programmable application processor. It includes high-performance, analog, and digital audio codecs, speaker driver, advanced power management, and flexible interfaces including interintegrated circuit sound (I^2S), universal asynchronous receiver transmitter (UART), and programmable input/output (PIO).

An application-dedicated Developer Processor and a system Firmware Processor run code from an external quad serial peripheral interface (QSPI) flash. Both processors have tightly coupled memory (TCM) and an on-chip cache for performance while executing from external flash memory. The system Firmware Processor provides functions developed by Goodocom Technologies Confidential, Ltd. The Developer processor provides flexibility to the product designer to customize their product.

The Audio subsystem contains a programmable Kalimba core running Goodocom® Kymera™ system DSP architecture framework from read only memory (ROM). A range of audio processing capabilities are provided from ROM which are configurable in fully flexible audio graphs.

The flexibility provided by the programmable applications processor plus the ability to configure the audio processor enables manufacturers to easily differentiate products with new features.

GOC-QF040 is driven by a flexible, software platform with powerful integrated development environment (IDE) support.

1.1 Module Block Diagram

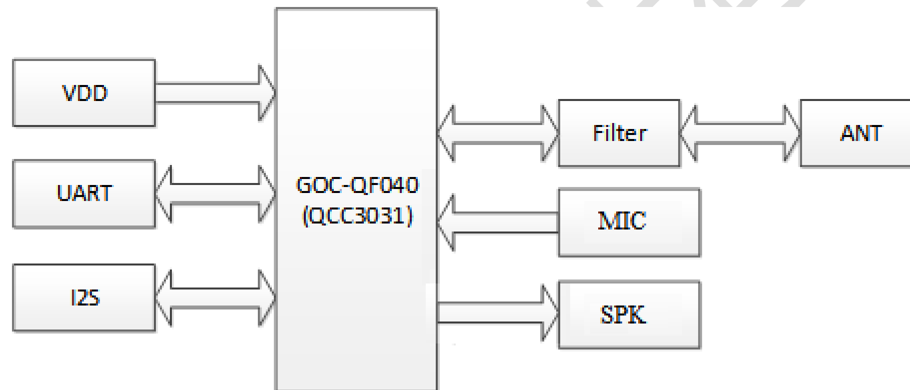


Figure 1: Module Block Diagram

1.2 Features

- High-performance programmable Bluetooth® stereo audio SoC with aptX™ audio
- Supports Bluetooth V5.0 including Bluetooth low energy 2 Mbps
- Fully qualified single-chip dual-mode Bluetooth V5.0 system
- Tri-core processor architecture with low power for extended battery life
- Qualified to Bluetooth® V5.0 specification
- Firmware Processor for system
- Flexible QSPI flash programmable platform
- Advanced audio algorithms
- High-performance 24-bit stereo audio interface
- Digital and analog microphone interfaces
- 1-mic cVc speaker noise reduction and echo cancellation technology
- aptX, aptX HD, aptX Low Latency, SBC, and AAC audio codecs support
- Integrated PMU: Dual SMPS for system/digital circuits, Integrated Li-ion battery charger
- Qualified to Bluetooth v5.0 specification including 2 Mbps Bluetooth low energy (Production parts)
- Bluetooth, Bluetooth low energy, and mixed topologies supported

- Class 3 support
- Programmable audio master clock (MCLK)
- Dual analog inputs configurable as single ended line inputs or, unbalanced or balanced analog microphone inputs:
  - SNR single-ended: 101 dBA typ.
  - THD+N single-ended: -85 dB typ.
- A UART interface
- Green (restriction of hazardous substances (RoHS) compliant and no antimony or halogenated flame retardants)

1.3 Application

- Wireless speakers

2. Main Specification Instruction

Production	Bluetooth Module
Type	GOC-QF040
Standard	Bluetooth V5.0
IC	QCC3031
Frequency Range	2.402~2.480GHz ISM Band
Modulation Method	GFSK, π/4-DQPSK,8DPSK
Max speed for transfer	Asynchronous: 723.2kbps/57.6kbps Synchronous: 433.9kbps/433.9kbps
Hop	1600hops/sec, 1MHz channel space
Output impedance	50 ohms
Crystal Frequency	32MHz
Outer interface	UART, I2S, Speaker, Microphone
Apply to Bluetooth instructions	A2DP AVRCP HFP HSP SPP APTX
Range for working distance	10 meters
Receiving Sensitivity	-90dBm
Emissive power	<4dBm
Size	32.50mm *24.07mm *3.14mm.
Power Voltage	5V supply voltage typically
Working Current	20mA
Standby Current	2mA
Storage temperature	-40 ℃ to +85 ℃
Temperature Range	-40 ℃ to +85 ℃
Humidity Range	10%~90% Non-Condensing

Table 1: Main Specification Instruction

3. Pin Diagram And Description

3.1 Pin Diagram

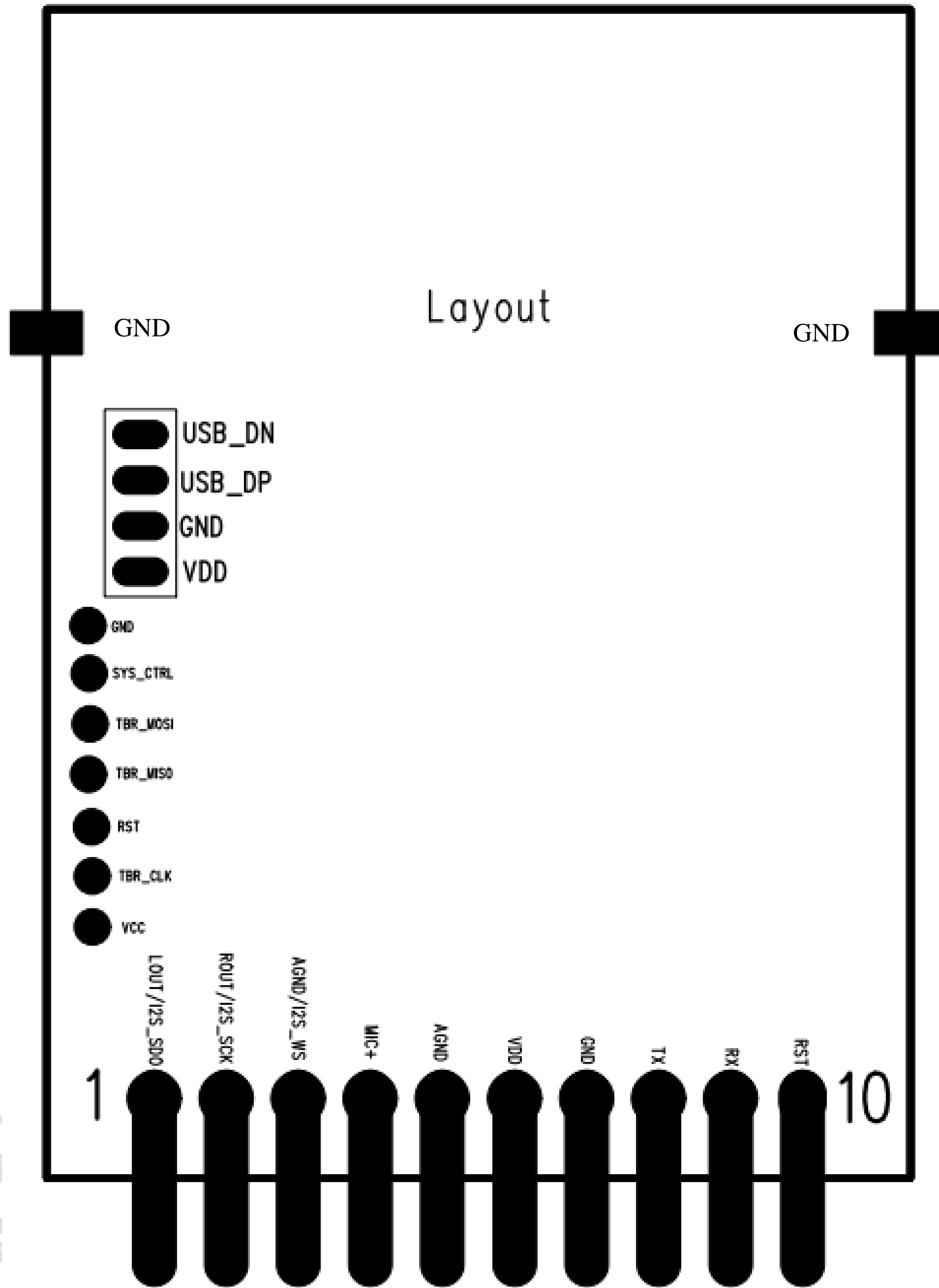


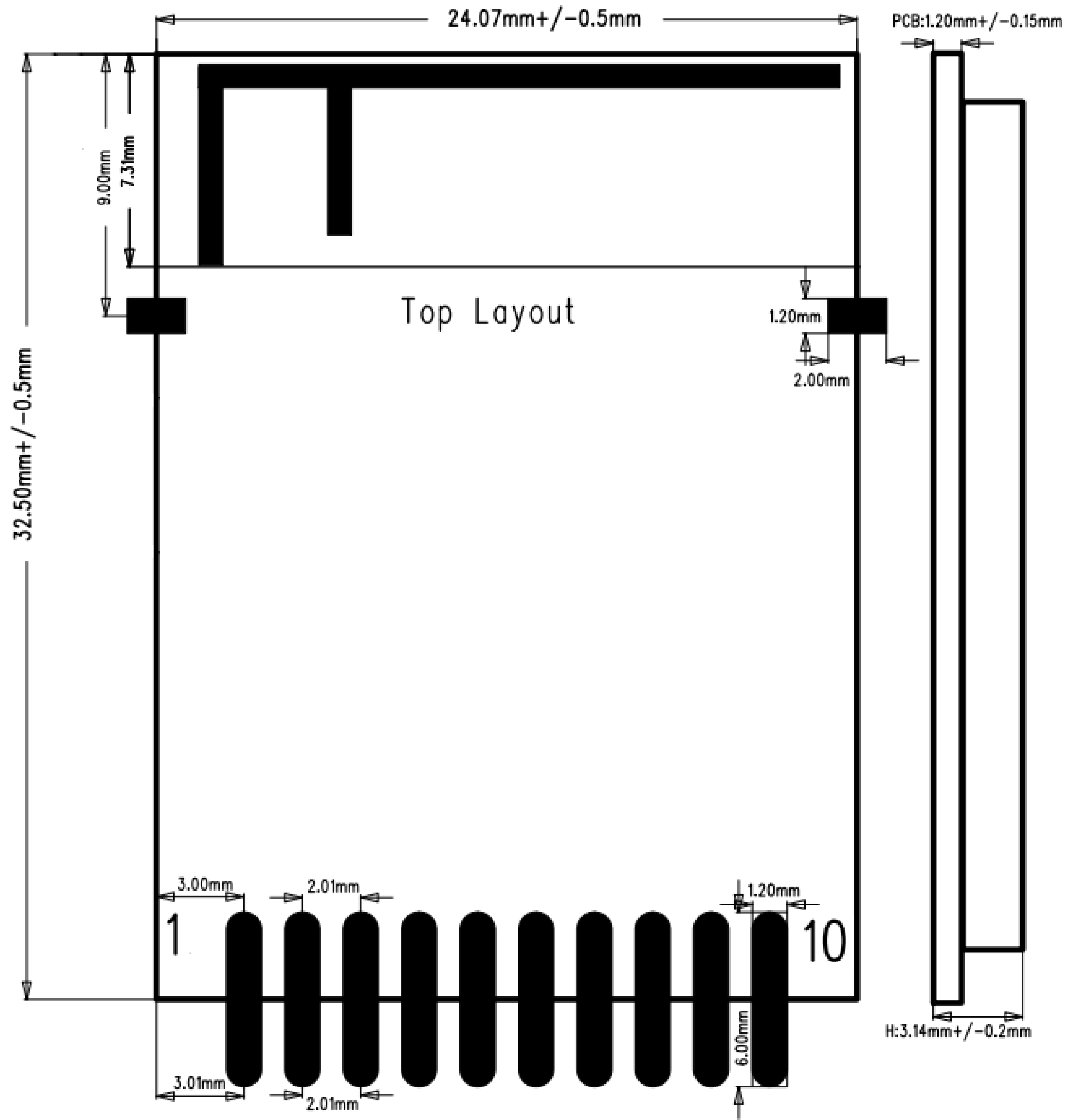
Figure 2: GOC-QF040 Pin Diagram

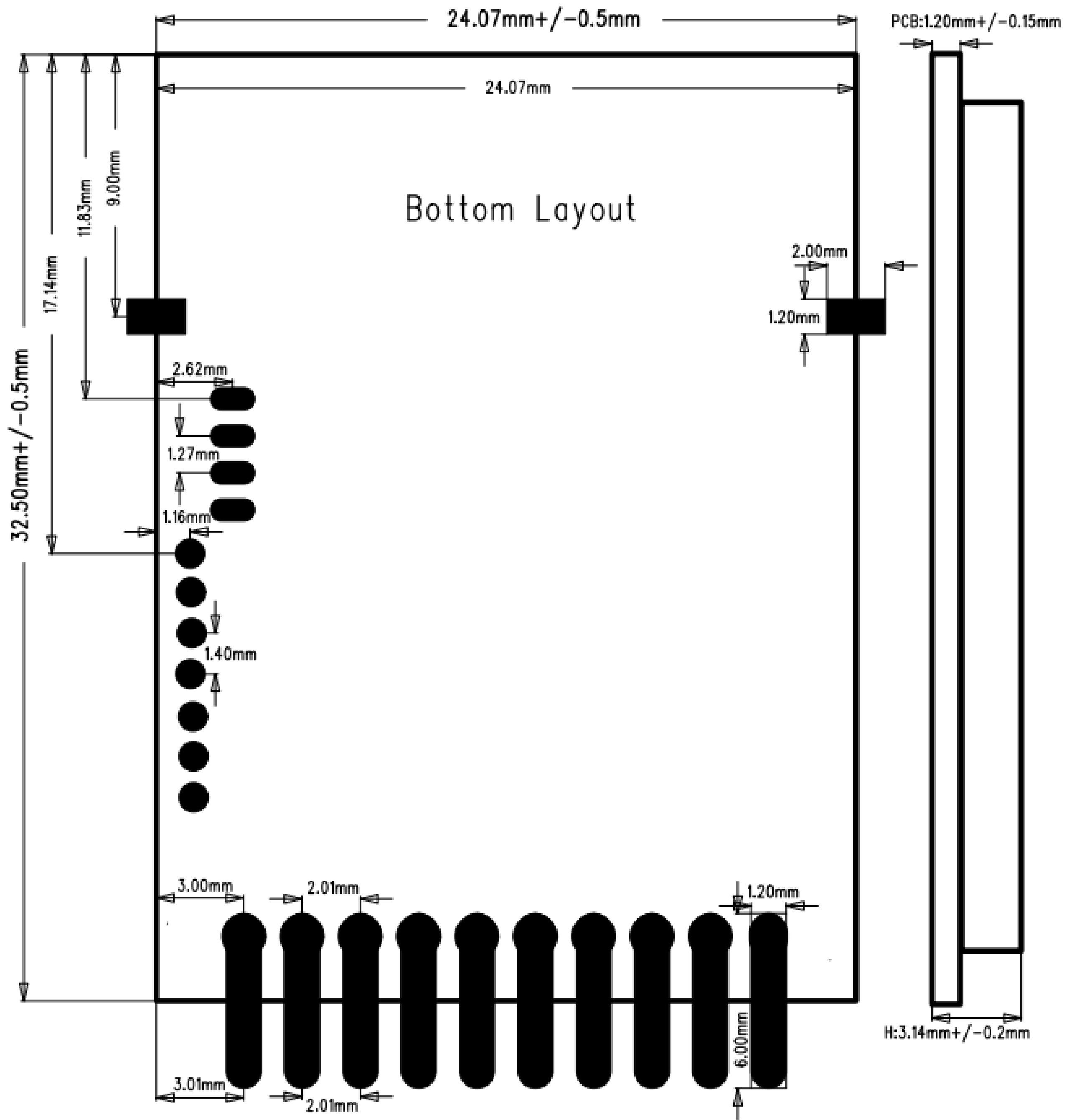
3.2 Pin Description

Pin	Pin Name	Pad Type	Description
1	LOUT/I2S_SDO	Output	Headphone/speaker differential left output/ I2S_SDO.
2	ROUT/I2S_SCK	Output	Headphone/speaker differential right output/I2S_SCK.
3	AGND/I2S_WS	AGND	Analog Ground /I2S_WS
4	MIC+	Input	Microphone differential input
5	AGND	AGND	Analog Ground
6	VDD	POWER	5V Supply voltage
7	GND	GND	Ground
8	TX	Input/Output	UART_TX
9	RX	Input/Output	UART_RX
10	RST	Input/Output	Bluetooth reset
11	VCC	POWER	3.3V Supply voltage(Debug interface)
12	TBR_CLK	-	Debug interface
13	RST	-	Debug interface
14	TBR_MISO	-	Debug interface
15	TBR_MOSI	-	Debug interface
16	TBR_CTRL	-	Debug interface
17	GND	GND	Ground
18	VDD	POWER	5V Supply voltage(Debug interface)
19	GND	GND	Ground
20	USB_DP	-	Debug interface
21	USB_DN	-	Debug interface
22	GND	GND	Ground
23	GND	GND	Ground

Table 2: Pin Description

3.3 PCB Layout Footprint





Note: Outter hole radius 0.75mm
Dirll hole size 0.8mm

Figure 3: PCB Layout Footprint

4. I²S Interface

GOC-QF040 provides a standard I²S/PCM interface capable of operating at up to a 192 kHz sample rate. The I²S port is highly configurable, and has the following options:

- ■ Master (generate CLK and WS) or Slave (receive CLK and WS)
- ■ Word Select polarity
- ■ Left or right justification
- ■ Sign extension / zero pad
- ■ Optional 1-bit period delay on WS to start of channel data
- ■ 13/16/24-bit per sample
- ■ Up to four slots per frame

NOTE:In multislot operation with 3 or 4 slots per frame, data padding to 32 bits within slots is not possible.

4.1 I²S Master Mode Timing Diagram

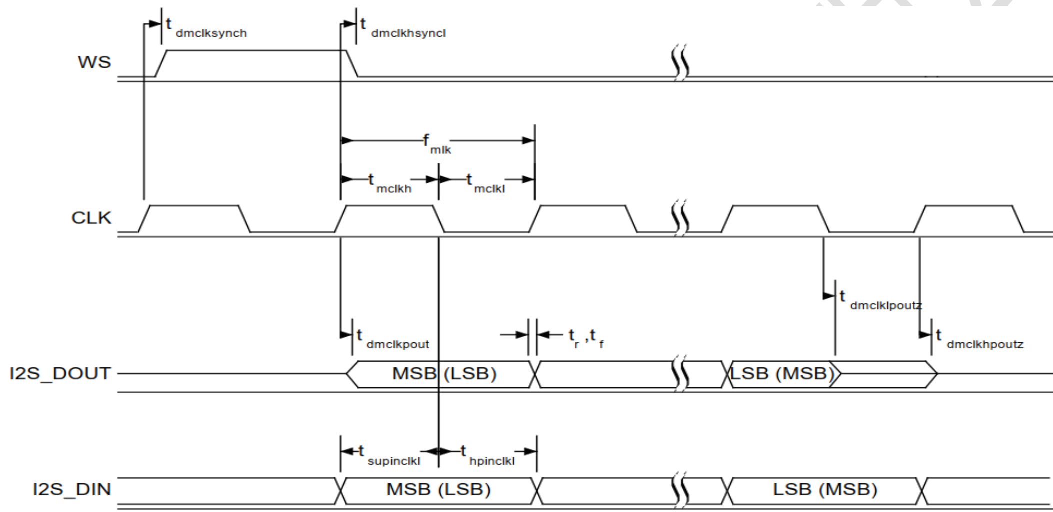


Figure 4: I²S master mode timing diagram

Symbol	Parameter	Min	Typ	Max	Unit
$t_{dmclksynch}$	Delay time from I2S_CLK high to I2S_SYNC high	-	-	20	ns
$t_{dmclkpout}$	Delay time from I2S_CLK high to valid I2S_OUT	-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from I2S_CLK high to I2S_SYNC low	-	-	20	ns
$t_{dmclklpoutz}$	Delay time from I2S_CLK low to I2S_OUT high impedance	-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from I2S_CLK high to I2S_OUT high impedance	-	-	20	ns
$t_{supinclkl}$	Set-up time for I2S_IN valid to I2S_CLK low	-	-	20	ns
$t_{hpinclkl}$	Hold time for I2S_CLK low to I2S_IN invalid	0	-	-	ns

Table 3: I²S master mode timing diagram symbols

4.2 I²S Slave Mode Timing Diagram

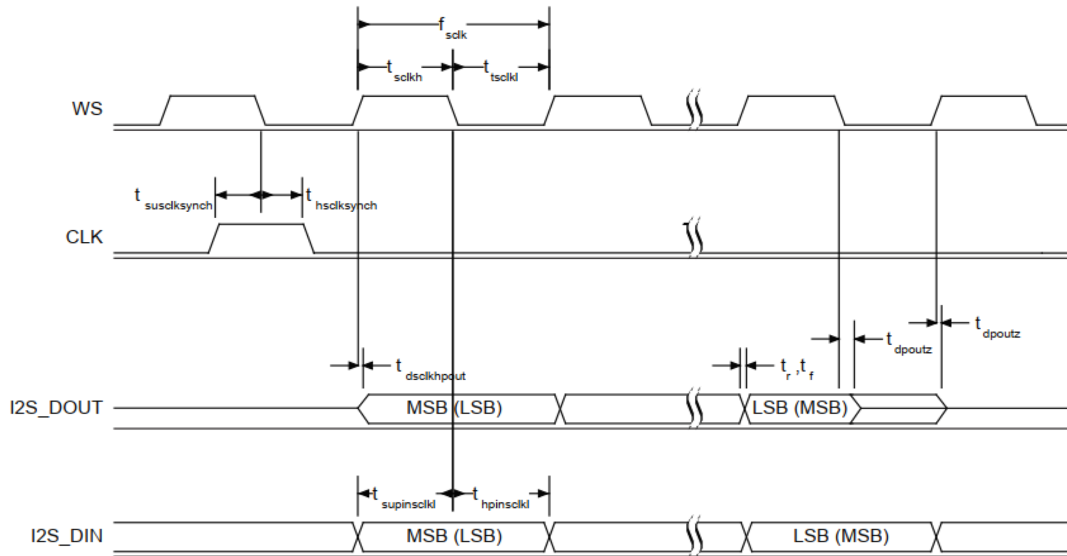


Figure 5: I^2S slave mode timing diagram

Symbol	Parameter	Min	Typ	Max	Unit
$t_{hsclksynch}$	Hold time from I2S_CLK low to I2S_SYNC high	5	-	-	ns
$t_{susclksynch}$	Set-up time for I2S_SYNC high to I2S_CLK low	15	-	-	ns
$t_{dsclkhpout}$	Delay time from CLK high to I2S_OUT valid data	-	-	20	ns
t_{dpoutz}	Delay time from I2S_SYNC or I2S_CLK low, whichever is later, to I2S_OUT data line high impedance	-	-	20	ns
$t_{supinsclkl}$	Set-up time for I2S_IN valid to CLK low	15	-	-	ns
$t_{hpinsclkl}$	Hold time for I2S_CLK low to I2S_IN invalid	5	-	-	ns

Table 4: I^2S slave mode timing diagram symbols

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Ratings	Min	Typical	Max
VDD	4.75V	5V	5.25V

Table 5: Absolute Maximum Ratings

5.2 Recommended Operating Conditions

Working Conditions	Min	Typical	Max
Storage temperature	-40 ℃	/	+85 ℃
Operating temperature	-40 ℃	20 ℃	+85 ℃
VDD	4.75V	5V	5.25V

Table 6: Recommended Operating Conditions

6. Recommended Reflow Profile

Referred to IPC/JEDEC standard.
Peak package body temperature :<260 ℃.
Time of peak temperature for Pb-free assembly : 5~10sec.

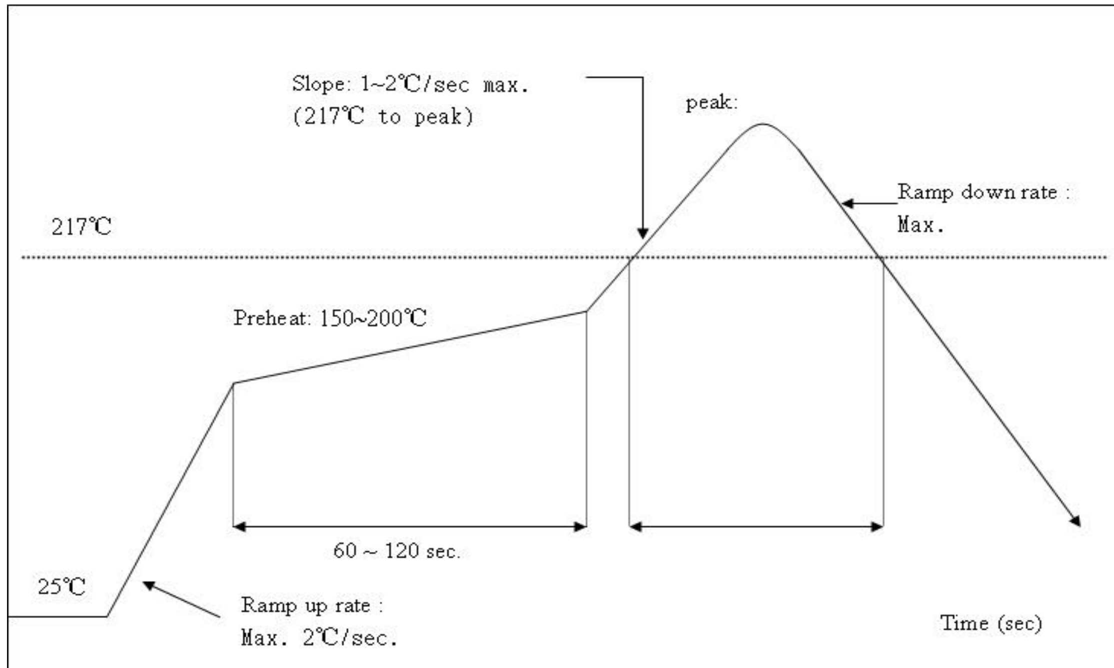


Figure 6: Solder Reflow Profile

7. PCB Layout Recommendation

7.1 Antenna

Antenna trace impedance should be adjusted to 50ohm.The area above(or under)the RF antenna trace should be free from other traces.

7.2 HCI UART Lines Layout Guideline

The following HCI line routing must obey the following rule to prevent overshoot/undershoot, as these lines drive 4 ~ 8mA
UART_RX
UART_TX
The route length of these signals be less than 15 cm and the line impedance be less than 50Ω.

7.3 Power Trace Lines Layout Guideline

VDD Trace Width: 30mil

7.4 Ground Lines Layout Guideline

A Complete Ground in Ground Layer.
Add Ground Through Holes to GOC-QF040 Module Ground Pads
Decoupling Capacitors close to GOC-QF040 Module Power and Ground Pads

8. Module Part Number Description

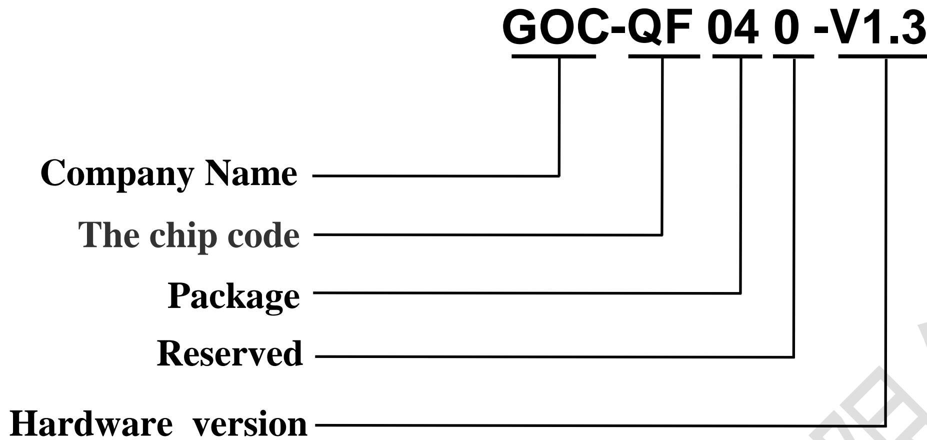


Figure 7: Module Part Number Description

For a list of available options (e.g. package, packing) and orderable part numbers or for further information on any aspect of this device, please go to www.goodocom.com or contact the GOODOCOM Sales Office nearest to you.

9. Ordering Information

Part Number	Description	Remark
GOC-QF040 V1.3	Bluetooth module	

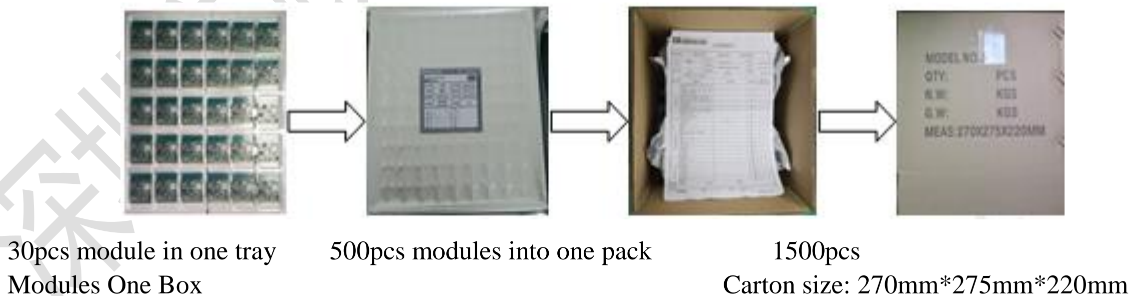
Table 7: Ordering information

10. Packaging Information

10.1 Net Weight

The module net weight: 2.5g±0.3g

10.2 Package



30pcs module in one tray 500pcs modules into one pack 1500pcs Modules One Box
Carton size: 270mm*275mm*220mm

10.3 Storage Requirements

1）Temperature: 22~28 ℃;
2 ）Humidity: <70%（ RH）;
Vacuum packed and sealed in good condition to ensure 12 months of welding.

10.4 Humidity Sensitive Characteristic

1） MSL: 3 level

2） Once opened, SMT within 168 hours in the condition of temperature: 22~28 ℃ and humidity<60%(RH).

3） Handling, storage, and processing should follow IPC/JEDECJ-STD-033

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